The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

~~a pixel portion comprising a plurality of pixels;~~

a signal line driver circuit; ~~and~~

an output switching circuit connected to the signal line driver circuit; and

a pixel portion comprising a plurality of pixels and connected to the output switching circuit,

wherein each of the plurality of pixels comprises a sensor portion and a light emitting element portion,

wherein the signal driver circuit outputs a timing signal to the output switching circuit, and

wherein the output switching circuit outputs different signals to the sensor portion and to the light emitting element portion.

2-4. (Canceled)

5. (Currently Amended) A semiconductor device comprising:

a pixel portion comprising a plurality of pixels;

a signal line driver circuit; and

an output switching circuit,

wherein each of the plurality of pixels comprises a sensor portion and a light emitting element portion,

wherein the output switching circuit comprises a first logical circuit and a second logical circuit,

~~wherein a first signal line is connected to one of the first logical circuit and second logical circuit, and a second signal line is connected to the other,~~

wherein the first logic circuit is connected to the sensor portion via a first signal

line and the second logic circuit is connected to the light emitting portion via a second signal line,

wherein the signal line driver circuit outputs a timing signal to the first logical circuit and to the second logical circuit,

~~wherein one of the first logical circuit and the second logical circuit outputs a first signal to the first signal line, and the other outputs a second signal to the second signal line, and~~

~~wherein the first signal is different from the second signal~~.

6. (Currently amended) A semiconductor device comprising:

a pixel portion comprising a plurality of pixels;

a signal line driver circuit; and

an output switching circuit,

wherein each of the plurality of pixels comprises a sensor portion and a liquid crystal element portion,

wherein the output switching circuit comprises a first logical circuit and a second logical circuit,

~~wherein a first signal line is connected to one of the first logical circuit and second logical circuit, and a second signal line is connected to the other,~~

wherein the first logic circuit is connected to the sensor portion via a first signal line and the second logic circuit is connected to the liquid crystal portion via a second signal line,

wherein the signal line driver circuit outputs a timing signal to the first logical circuit and to the second logical circuit,

~~wherein one of the first logical circuit and the second logical circuit outputs a first signal to the first signal line, and the other outputs a second signal to the second signal line, and~~

~~wherein the first signal is different from the second signal~~.

7-8. (Canceled)

9. (Currently Amended) A semiconductor device comprising:

a pixel portion comprising a plurality of pixels;

a signal line driver circuit; and

an output switching circuit connected to the signal line driver circuit,

wherein each of the plurality of pixels comprises a sensor portion and a light emitting element portion,

wherein the sensor portion comprises a first TFT, and the light emitting element portion comprises a second TFT,

wherein the output switching circuit comprises a first logical circuit and a second logical circuit,

~~wherein a first signal line is connected to one of the first logical circuit and the second logical circuit, a second signal line is connected to the other,~~

~~wherein the first TFT is connected to the first signal line, and the second TFT is connected to the second signal line,~~

wherein the first logic circuit is connected to the first TFT via a first signal line and the second logic circuit is connected to the second TFT via a second signal line,

wherein the signal line driver circuit outputs a timing signal to the first logical circuit and to the second logical circuit~~,~~

~~wherein one of the first logical circuit and the second logical circuit outputs a first signal to the first signal line, and the other outputs a second signal to the second signal line,~~

~~wherein the first signal line outputs the first signal to the first TFT, and the second signal line outputs the second signal to the second TFT, and~~

~~wherein the first signal is different from the second signal~~.

10. (Currently Amended) A semiconductor device comprising:

a pixel portion comprising a plurality of pixels;

a signal line driver circuit; and

an output switching circuit connected to the signal line driver circuit,

wherein each of the plurality of pixels comprises a sensor portion and a liquid crystal element portion,

wherein the sensor portion comprises a first TFT, and the liquid crystal element portion comprises a second TFT,

wherein the output switching circuit comprises a first logical circuit and a second logical circuit,

~~wherein a first signal line is connected to one of the first logical circuit and the second logical circuit, a second signal line is connected to the other,~~

~~wherein the first TFT is connected to the first signal line, and the second TFT is connected to the second signal line,~~

wherein the first logic circuit is connected to the first TFT via a first signal line and the second logic circuit is connected to the second TFT via a second signal line,

wherein the signal line driver circuit outputs a timing signal to the first logical circuit and to the second logical circuit~~,~~

~~wherein one of the first logical circuit and the second logical circuit outputs a first signal to the first signal line, and the other outputs a second signal to the second signal line,~~

~~wherein the first signal line outputs the first signal to the first TFT, and the second signal line outputs the second signal to the second TFT, and~~

~~wherein the first signal is different from the second signal~~.

11. (Currently Amended) A semiconductor device comprising:

a pixel portion having a plurality of pixels;

a signal line driver circuit; and

an output switching circuit connected to the signal line driver circuit,

wherein each of the plurality of pixels comprises a sensor portion and a light emitting element portion,

wherein the sensor portion comprises a first TFT, and the light emitting element portion comprises a second TFT,

wherein the output switching circuit comprises a first logical circuit and a second logical circuit,

~~wherein a first signal line is connected to one of the first logical circuit and the second logical circuit, and a second signal line is connected to the other,~~

~~wherein the first TFT is connected to the first signal line, and the second TFT is connected to the second signal line,~~

wherein the first logic circuit is connected to the first TFT via a first signal line and the second logic circuit is connected to the second TFT via a second signal line,

wherein the signal line driver circuit outputs a timing signal to the first logical circuit and to the second logical circuit,

wherein light emitted from the light emitting element portion is reflected by a subject and irradiated to the sensor portion, and the sensor portion generates an image signal from the irradiated light~~,~~

~~wherein one of the first logical circuit and the second logical circuit outputs a pulse signal to the first signal line, and the other outputs an on signal to the second signal line, and~~

~~wherein the first signal line outputs the pulse signal to the first TFT, and the second signal line outputs the on signal to the second TFT~~.

12. (Canceled)

13. (Currently Amended) A semiconductor device comprising:

a pixel portion comprising a plurality of pixels;

a signal line driver circuit;

an output switching circuit connected to the signal line driver circuit; and

one of a back light and a front light,

wherein each of the plurality of pixels comprises a sensor portion and a liquid crystal element portion,

wherein the sensor portion comprises a first TFT, and the liquid crystal element portion comprises a second TFT,

wherein the output switching circuit comprises a first logical circuit and a second logical circuit,

~~wherein a first signal line is connected to one of the first logical circuit and the second logical circuit, and a second signal line is connected to the other,~~

~~wherein the first TFT is connected to the first signal line, and the second TFT is~~

~~connected to the second signal line,~~

wherein the first logic circuit is connected to the first TFT via a first signal line and the second logic circuit is connected to the second TFT via a second signal line,

wherein the signal line driver circuit outputs a timing signal to the first logical circuit and to the second logical circuit,

wherein light emitted from one of the back light and the front light is reflected by a subject and irradiated to the sensor portion, and the sensor portion generates an image signal from the irradiated light, and

wherein ~~one~~ the first logical circuit ~~and the second logical circuit~~ outputs a pulse signal to the first signal line, and ~~the other~~ the second logic circuit outputs an on signal to the second signal line~~, and~~

~~wherein the first signal line outputs the pulse signal to the first TFT, and the second signal line outputs the on signal to the second TFT~~.

14-16. (Canceled)

17. (Original) A semiconductor device according to claim 5, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

18. (Original) A semiconductor device according to claim 6, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

19-20. (Canceled)

21. (Original) A semiconductor device according to claim 9, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

22. (Original) A semiconductor device according to claim 10, wherein one of the

first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

23. (Original) A semiconductor device according to claim 11, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

24. (Canceled)

25. (Original) A semiconductor device according to claim 13, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

26-28. (Canceled)

29. (Original) A semiconductor device according to claim 5, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

30. (Original) A semiconductor device according to claim 6, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

31-32. (Canceled)

33. (Original) A semiconductor device according to claim 9, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

34. (Original) A semiconductor device according to claim 10, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR

circuit.

35. (Original) A semiconductor device according to claim 11, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

36. (Canceled)

37. (Original) A semiconductor device according to claim 13, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

38-40. (Canceled)

41. (Original) A semiconductor device according to claim 5, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

42. (Original) A semiconductor device according to claim 6, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

43-44. (Canceled)

45. (Original) A semiconductor device according to claim 9, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

46. (Original) A semiconductor device according to claim 10, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

47. (Original) A semiconductor device according to claim 11, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

48. (Canceled)

49. (Original) A semiconductor device according to claim 13, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

50-52. (Canceled)

53. (Original) A semiconductor device according to claim 5, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

54. (Original) A semiconductor device according to claim 6, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

55-56. (Canceled)

57. (Original) A semiconductor device according to claim 9, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

58. (Original) A semiconductor device according to claim 10, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

59. (Original) A semiconductor device according to claim 11, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

60. (Canceled)

61. (Original) A semiconductor device according to claim 13, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

62. (Canceled)

63. (Original) A semiconductor device according to claim 5, wherein one of the first signal line and the second signal line is a selection signal line, and the other is a sensor selection signal line.

64. (Original) A semiconductor device according to claim 9, wherein one of the first signal line and the second signal line is a selection signal line, and the other is a sensor selection signal line.

65. (Original) A semiconductor device according to claim 11, wherein one of the first signal line and the second signal line is a selection signal line, and the other is a sensor selection signal line.

66. (Canceled)

67. (Original) A semiconductor device according to claim 5, wherein one of the first signal line and the second signal line is a reset signal line, and the other is a sensor reset signal line.

68. (Original) A semiconductor device according to claim 9, wherein one of the

first signal line and the second signal line is a reset signal line, and the other is a sensor reset signal line.

69. (Original) A semiconductor device according to claim 11, wherein one of the first signal line and the second signal line is a reset signal line, and the other is a sensor reset signal line.

70. (Canceled)

71. (Original) A semiconductor device according to claim 5, wherein one of the first signal line and the second signal line is a selection signal line, and the other is a sensor reset signal line.

72. (Original) A semiconductor device according to claim 9, wherein one of the first signal line and the second signal line is a selection signal line, and the other is a sensor reset signal line.

73. (Original) A semiconductor device according to claim 11, wherein one of the first signal line and the second signal line is a selection signal line, and the other is a sensor reset signal line.

74. (Canceled)

75. (Original) A semiconductor device according to claim 5, wherein one of the first signal line and the second signal line is a reset signal line, and the other one is a sensor selection signal line.

76. (Original) A semiconductor device according to claim 9, wherein one of the first signal line and the second signal line is a reset signal line, and the other one is a sensor selection signal line.

77. (Original) A semiconductor device according to claim 11, wherein one of the

first signal line and the second signal line is a reset signal line, and the other one is a sensor selection signal line.

78. (Canceled)

79. (Original) A semiconductor device according to claim 6, wherein one of the first signal line and the second signal line is a liquid crystal selection signal line, and the other is a sensor selection signal line.

80. (Original) A semiconductor device according to claim 10, wherein one of the first signal line and the second signal line is a liquid crystal selection signal line, and the other is a sensor selection signal line.

81. (Original) A semiconductor device according to claim 13, wherein one of the first signal line and the second signal line is a liquid crystal selection signal line, and the other is a sensor selection signal line.

82. (Canceled)

83. (Original) A semiconductor device according to claim 6, wherein one of the first signal line and the second signal line is a liquid crystal selection signal line, and the other is a sensor reset signal line.

84. (Original) A semiconductor device according to claim 10, wherein one of the first signal line and the second signal line is a liquid crystal selection signal line, and the other is a sensor reset signal line.

85. (Original) A semiconductor device according to claim 13, wherein one of the first signal line and the second signal line is a liquid crystal selection signal line, and the other is a sensor reset signal line.

86-87. (Canceled)

88. (Original) A semiconductor device according to claim 9, wherein one of the first TFT and the second TFT is a selection TFT, and the other is a sensor selection TFT.

89. (Original) A semiconductor device according to claim 11, wherein one of the first TFT and the second TFT is a selection TFT, and the other is a sensor selection TFT.

90-91. (Canceled)

92. (Original) A semiconductor device according to claim 9, wherein one of the first TFT and the second TFT is a selection TFT, and the other is a sensor reset TFT.

93. (Original) A semiconductor device according to claim 11, wherein one of the first TFT and the second TFT is a selection TFT, and the other is a sensor reset TFT.

94-95. (Canceled)

96. (Original) A semiconductor device according to claim 9, wherein one of the first TFT and the second TFT is a reset TFT, and the other is a sensor reset TFT.

97. (Original) A semiconductor device according to claim 11, wherein one of the first TFT and the second TFT is a reset TFT, and the other is a sensor reset TFT.

98-99. (Canceled)

100. (Currently Amended) A semiconductor device according to claim 9, wherein one of the first TFT and the second TFT is a reset TFT, and the other is [s] a sensor selection TFT.

101. (Currently Amended) A semiconductor device according to claim 11, wherein one of the first TFT and the second TFT is a reset TFT, and the other is [s] a sensor selection TFT.

102-103. (Canceled)

104. (Original) A semiconductor device according to claim 10, wherein one of the first TFT and the second TFT is a liquid crystal selection TFT, and the other is a sensor selection TFT.

105. (Original) A semiconductor device according to claim 13, wherein one of the first TFT and the second TFT is a liquid crystal selection TFT, and the other is a sensor selection TFT.

106-107. (Canceled)

108. (Original) A semiconductor device according to claim 10, wherein one of the first TFT and the second TFT is a liquid crystal selection TFT, and the other one is a sensor reset TFT.

109. (Original) A semiconductor device according to claim 13, wherein one of the first TFT and the second TFT is a liquid crystal selection TFT, and the other one is a sensor reset TFT.

110-112. (Canceled)

113. (Currently Amended) A semiconductor device according to [any one of] claim 5, wherein an output terminal of the first logical circuit is connected to at least one inverter circuit.

114. (Currently Amended) A semiconductor device according to [any one of]

claim 6, wherein an output terminal of the first logical circuit is connected to at least one inverter circuit.

115-116. (Canceled)

117. (Currently Amended) A semiconductor device according to [any one of] claim 9, wherein an output terminal of the first logical circuit is connected to at least one inverter circuit.

118. (Currently Amended) A semiconductor device according to [any one of] claim 10, wherein an output terminal of the first logical circuit is connected to at least one inverter circuit.

119. (Currently Amended) A semiconductor device according to [any one of] claim 11, wherein an output terminal of the first logical circuit is connected to at least one inverter circuit.

120. (Canceled)

121. (Currently Amended) A semiconductor device according to [any one of] claim 13, wherein an output terminal of the first logical circuit is connected to at least one inverter circuit.

122-124. (Canceled)

125. (Original) A semiconductor device according to claim 5, wherein an output terminal of the second logical circuit is connected to at least one inverter circuit.

126. (Original) A semiconductor device according to claim 6, wherein an output terminal of the second logical circuit is connected to at least one inverter circuit.

127-128. (Canceled)

129. (Original) A semiconductor device according to claim 9, wherein an output terminal of the second logical circuit is connected to at least one inverter circuit.

130. (Original) A semiconductor device according to claim 10, wherein an output terminal of the second logical circuit is connected to at least one inverter circuit.

131. (Original) A semiconductor device according to claim 11, wherein an output terminal of the second logical circuit is connected to at least one inverter circuit.

132. (Canceled)

133. (Original) A semiconductor device according to claim 13, wherein an output terminal of the second logical circuit is connected to at least one inverter circuit.

134. (Canceled)

135. (Original) A semiconductor device according to claim 1, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a reset TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

136. (Canceled)

137. (Original) A semiconductor device according to claim 5, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a reset TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

138. (Canceled)

139. (Original) A semiconductor device according to claim 9, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a reset TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

140. (Original) A semiconductor device according to claim 11, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a reset TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

141. (Canceled)

142. (Original) A semiconductor device according to claim 1, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

143. (Canceled)

144. (Original) A semiconductor device according to claim 5, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

145. (Canceled)

146. (Original) A semiconductor device according to claim 9, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

147. (Original) A semiconductor device according to claim 11, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

148-150. (Canceled)

151. (Currently Amended) A semiconductor device according to claim 6, wherein each of the plurality of pixels comprises a liquid crystal element, a liquid crystal selection TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

152. (Canceled)

153. (Currently Amended) A semiconductor device according to claim 10, wherein each of the plurality of pixels comprises a liquid crystal element, a liquid crystal selection TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

154. (Currently Amended) A semiconductor device according to claim 13, wherein each of the plurality of pixels comprises a liquid crystal element, a liquid crystal selection TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

155. (Canceled)

156. (Original) A semiconductor device according to claim 1, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

157-159. (Canceled)

160. (Original) A semiconductor device according to claim 5, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

161. (Original) A semiconductor device according to claim 6, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

162-163. (Canceled)

164. (Original) A semiconductor device according to claim 9, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

165. (Original) A semiconductor device according to claim 10, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

166. (Original) A semiconductor device according to claim 11, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

167. (Canceled)

168. (Original) A semiconductor device according to claim 13, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

169. (Canceled)

170. (Original) A display device using a semiconductor device according to claim 1.

171-173. (Canceled)

174. (Original) A display device using a semiconductor device according to claim 5.

175. (Original) A display device using a semiconductor device according to claim 6.

176-177. (Canceled)

178. (Original) A display device using a semiconductor device according to claim 9.

179. (Original) A display device using a semiconductor device according to claim 10.

180. (Original) A display device using a semiconductor device according to claim 11.

181. (Canceled)

182. (Original) A display device using a semiconductor device according to claim 13.

183. (Canceled)

184. (Original) A scanner using a semiconductor device according to claim 1.

185-187. (Canceled)

188. (Original) A scanner using a semiconductor device according to claim 5.

189. (Original) A scanner using a semiconductor device according to claim 6.

190-191. (Canceled)

192. (Original) A scanner using a semiconductor device according to claim 9.

193. (Original) A scanner using a semiconductor device according to claim 10.

194. (Original) A scanner using a semiconductor device according to claim 11.

195. (Canceled)

196. (Original) A scanner using a semiconductor device according to claim 13.

197. (Canceled)

198. (Original) A portable information terminal using a semiconductor device according to claim 1.

199-201. (Canceled)

202. (Original) A portable information terminal using a semiconductor device according to claim 5.

203. (Original) A portable information terminal using a semiconductor device according to claim 6.

204-205. (Canceled)

206. (Original) A portable information terminal using a semiconductor device according to claim 9.

207. (Original) A portable information terminal using a semiconductor device according to claim 10.

208. (Original) A portable information terminal using a semiconductor device according to claim 11.

209. (Canceled)

210. (Original) A portable information terminal using a semiconductor device according to claim 13.

211-233. (Canceled)